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PRODUCTION MEASUREMENT OF FUZE COMPONENTS UNDER DYNAMIC STRESS.(U)
AUG 77 A J EISENBERGER, P KASZERMAN DAAB07-76-C-0032
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FIFTH QUARTERLY REPORT

PRODUCTION MEASUREMENT OF FUZE COMPONENTS UNDER DYNAMIC STRESS

11 May 1977 - 10 August 1977

CONTRACT NUMBER DAAB07-76-C-0032

PLACED BY

U.S. ARMY ELECTRONICS COMMAND
PROCUREMENT AND PRODUCTION DIRECTORATE
COMMUNICATION SYSTEMS PROCUREMENT BRANCH
FORT MONMOUTH, NEW JERSEY 07703

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PRODUCTION MEASUREMENT OF FUZE COMPONENTS UNDER DYNAMIC STRESS

FIFTH QUARTERLY REPORT

11 May 1977 - 10 August 1977

OBJECT OF STUDY: DEVELOPMENT OF A COMPUTER CONTROLLED AUTOMATIC TESTER, CAPABLE OF TESTING AND TRIMMING THICK FILM ADJUSTMENT CIRCUITS AT THE RATE OF 3,000/HOUR

CONTRACT NUMBER DAAB07-76-C-0032

PREPARED BY

ARTHUR J. EISENBERGER
PHILIP KASZERMAN

ABSTRACT

During the fifth quarter, the amplifier test simulator program was modified and incorporated into the real-time program. Input/output (i/o) routines were added and partially debugged. Computer control of the laser was achieved. An additional memory (32k) and a more sophisticated operating system were ordered for the computer.

Seventy-five amplifier boards were assembled and successfully tested. Additionally, 75 oscillator assemblies have been 90 percent completed. Purchase orders have been generated for the components of the oscillator test signal system (modulator).

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1. PURPOSE

The purpose of this program is to develop a dynamic test and correction system, capable of high-speed operation, for electronic assemblies. The circuits selected for verification under this contract are the oscillator and amplifier assemblies of the M732 fuze. The contract requires that 3,000 units of each assembly be delivered, of which 2,900 have been trimmed to meet the specifications. The required test rate is 3,000 an hour.

2. NARRATIVE AND DATA

2.1 INTRODUCTION

During the fifth quarter, the amplifier test simulation program was modified and incorporated into the real-time program. I/O routines were added and partially debugged. Computer control of the laser was achieved. An additional memory (32k) and a more sophisticated operating system were ordered for the computer.

Seventy-five boards were assembled and successfully tested. Additionally, 75 oscillator assemblies have been 90 percent completed. Purchase orders have been generated for the oscillator test signal system (modulator).

2.2 REDESIGNED FUZE

2.2.1 Fuze Prototype Fabrication

Amplifiers. - A total of 75 amplifier boards were assembled, of which 74 were tested and certified as operational (1 unit was used as a mechanical sample for fixturing purposes). Chip resistors were attached to 54 units as per the following schedule:

- 24-Cermalloy (SN: C1-1 through -24)
- 15-Electro Science Laboratories (SN: ESI-4, -6 through -15, -17 through -20)
- 15-Englehard (SN: EN-1, -3, -4, -6, -7, -9, -10, -12 through -19)

The remaining 15 units were tested without chip resistors mounted in place. All units performed satisfactorily. These prototypes will be laser trimmed in the next quarter.

All units have been tagged and characterized to permit tracking of chip resistor values through trimming and determination of resistance variation effects (see tables 1, 2, and 3).

Table 1. Test Data Prototype Amplifier Assembly (Dwg No. 06006404) - Cermalloy

Fuze Serial No.	I Max .32V	T_D 1.0-3.0V	HOB MID .22-.28V	HOB LOW .10-.18V	HOB HIGH .14-.24V	Noise Pass	Noise Fail	T_{INT} .4-.8V	R9 Value (ohms)	Remarks
C1-1	.254	1.824	.0875	.060	.039	✓		.694	652	
2	.266	1.905	.085	.049	.043	✓		.639	627	
3	.256	1.918	.082	.055	.038	✓		.652	623	
4	.256	1.902	.082	.050	.038	✓		.709	662	
5	.257	1.937	.080	.052	.033	✓		.745	644	
6	.262	1.990	.090	.058	.045	✓		.644	641	
7	.257	1.981	.0835	.053	.040	✓		.663	622	
8	.252	2.034	.0785	.055	.032	✓		.703	623	
9	.261	1.927	.0725	.046	.031	✓		.690	639	
10	.263	1.864	.075	.049	.032	✓		.666	643	
11	.251	1.862	.0825	.054	.039	✓		.674	646	
12	.258	1.920	.089	.056	.043	✓		.665	660	
13	.258	1.893	.0875	.053	.040	✓		.722	637	
14	.260	1.864	.080	.053	.035	✓		.617	616	
15	.258	2.045	.0785	.057	.033	✓		.690	625	
16	.250	1.945	.0955	.064	.046	✓		.733	664	
17	.261	1.927	.0745	.049	.030	✓		.765	638	
18	.252	1.889	.085	.056	.040	✓		.665	676	
19	.257	2.010	.0815	.049	.040	✓		.679	664	
20	.268	1.938	.082	.057	.035	✓		.708	654	
21	.252	1.985	.073	.046	.031	✓		.724	634	
22	.261	1.893	.0955	.057	.050	✓		.666	674	
23	.258	1.909	.0915	.053	.046	✓		.698	671	
24	.253	1.954	.086	.056	.042	✓		.724	690	
MEAN			0.08325	0.053625	0.038375				646.875	
STD DEV.			0.00638	0.004382	0.005531				19.933	

Note:

I = Amplifier Bias Current

T_D = Arming Time

HOB = Height of Burst

Noise = B+ Noise Test

T_{INT} = Integration Time

R9 = Resistance Value (see figure 5)

Each voltage value shown is directly proportional to the specific property being tested. See text for a further explanation of individual parameters.

Table 2. Test Data Prototype Amplifier Assembly (Dwg No. 06006404) - Electro Science Laboratories

Fuze Serial No.	I Max .32V	T_D 1.0-3.0V	HOB MID .22-.28V	HOB LOW .10-.18V	HOB HIGH .14-.24V	Noise Pass	Noise Fail	T_{INT} .4-.8V	R9 Value (ohms)	Remarks
ESL-1										
2										
3										
4	.269	1.884	.1045	.064	.058	✓		.657	759	
5										
6	.265	1.991	.108	.067	.060	✓		.628	782	
7	.257	1.841	.0935	.056	.049	✓		.704	739	
8	.249	1.915	.110	.071	.061	✓		.645	738	
9	.262	1.930	.093	.060	.046	✓		.693	774	
10	.259	1.985	.1185	.080	.065	✓		.625	774	
11	.255	1.934	.1065	.069	.056	✓		.684	775	
12	.259	1.982	.0995	.064	.051	✓		.643	728	
13	.261	1.906	.0925	.066	.044	✓		.586	751	
14	.253	1.941	.100	.067	.054	✓		.673	747	
15	.259	1.863	.0995	.064	.049	✓		.750	758	
16										
17	.262	1.866	.094	.061	.046	✓		.716	750	
18	.257	1.915	.114	.071	.064	✓		.640	779	
19	.259	1.990	.0965	.058	.050	✓		.661	777	
20	.260	1.869	.101	.064	.052	✓		.704	755	
MEAN			0.10207	0.06547	0.05367				759.07	
STD DEV.			0.00801	0.005939	0.006715				17.044	

Note:

I = Amplifier Bias Current
T_D = Arming Time
HOB = Height of Burst
Noise = B+ Noise Test
T_{INT} = Integration Time
R9 = Resistance Value (see figure 5)

Each voltage value shown is directly proportional to the specific property being tested.
See text for a further explanation of individual parameters.

Table 3. Test Data Prototype Amplifier Assembly (Dwg. No. 0600404) - Englehard

Fuze Serial No.	I Max .32V	T_D 1.0-3.0V	HOB MID .22-.28V	HOB LOW .10-.18V	HOB HIGH .14-.24V	Noise Pass	Noise Fail	T_{INT} .4-.8V	R9 Value (ohms)	Remarks
EN-1	.261	1.932	.099	.063	.054	✓		.582	705	
2										
3	.260	1.895	.097	.064	.049	✓		.622	676	
4	.269	1.902	.096	.056	.053	✓		.667	722	
5										
6	.263	1.873	.0895	.057	.044	✓		.704	694	
7	.264	1.930	.0965	.063	.048	✓		.673	703	
8										
9	.256	1.895	0.935	.057	.045	✓		.752	680	
10	.266	2.026	0.084	.056	.038	✓		.704	659	
11										
12	.268	1.959	.0935	.064	.046	✓		.641	704	
13	.252	2.046	.076	.039	.033	✓		.721	671	
14	.251	1.922	.091	.059	.048	✓		.654	674	
15	.254	1.911	.0845	.059	.039	✓		.692	656	
16	.255	1.854	.089	.063	.042	✓		.679	658	
17	.259	1.918	.067	.045	.025	✓		.715	558	
18	.260	1.975	.0945	.064	.048	✓		.673	664	
19	.253	2.033	.090	.063	.044	✓		.633	695	
MEAN			0.0893	0.05813	0.04373				674.6	
STD DEV.			0.008527	0.007318	0.0075826				38.033	

Note:

I = Amplifier Bias Current
T_D = Arming Time
HOB = Height of Burst
Noise = B+ Noise Test
T_{INT} = Integration Time
R9 = Resistance Value (see figure 5)

Each voltage value shown is directly proportional to the specific property being tested. See text for a further explanation of individual parameters.

Additional resistor chips have been produced from other substrates using the services of a laser machining house.

Tables 1, 2, and 3 summarize measurements made on the pretuned prototype amplifier boards described above using an in-house amplifier board tester for the M732 fuze. Seven tests are conducted during a normal production cycle:

- Bias current (I)
- Arming time (T_D)
- Height-of-Burst (HOB)
  - Mid frequency
  - Low frequency
  - High frequency
- B+ noise test
- Integration Time (T_{INT})

Bias current (I) is the overall current supplied by a 30.00-Vdc power supply to each test amplifier. Arming time (T_D) is the time needed to charge the fire pulse energy storage capacitor.

Three HOB measurements are performed; one each at low, mid, and high doppler frequencies.

A noise measurement is conducted where a 100mVrms audio tone is impressed in series with the power supply for a specified length of time, while the amplifier board fire pulse output port is monitored. If a fire pulse appears, the unit fails this test. If no fire pulse is observed, the unit is considered good.

Integration time (T_{INT}) is a fundamental property of the amplifier board integrator circuit.

Note that the limits presented are all in volts, even though actual units are current, time, voltage, or distance. The specific correlation factors have been left out for security purposes.

All units are within the bounds specified at the top of each column with the exception of the HOB voltages, which are all below the specified range at each doppler frequency. This undershooting is the result of the lower than normal values of R9 which, as yet, have not been laser trimmed. As R9 values increase, the test voltages will increase to the nominal values at each doppler frequency (Low - 0.14V; Mid - 0.25V; High - 0.19Vdc).

2.2.2 Prototype Oscillators

Seventy-five prototype Formed Antennas (Dwg No. 06006416), and Oscillator Printed Circuit Boards (pcb) (Dwg No. 06006407), were delivered during this quarter for evaluation. The antennas were found to be unsatisfactory and were rejected.[1] A new lot of 63 units were received at the end of the quarter and will be assembled during the next quarter. Two selected units of the initial lot, however, were assembled and electrically tested in an existing oscillator tester. These oscillators performed similarly to the original Harry Diamond Laboratory (HDL) designed units. Detailed electrical measurements of the new prototype oscillator assemblies will be made after assembly of the formed antennas. A systematic evaluation of these modified oscillators will be performed.

2.2.3 Oscillator Chip Capacitor

Two separate binary-valued capacitance designs were constructed and evaluated during the present quarter. Individual plate size dimensions were based on different theoretical and experimental criteria of fringing capacitance. Figure 1 shows an enlarged version of the artwork for the design based on an experimental estimate of fringing capacity. The other design, based on a theoretical fringing criteria, looks similar except for slightly different pad size dimensions for each "bit".

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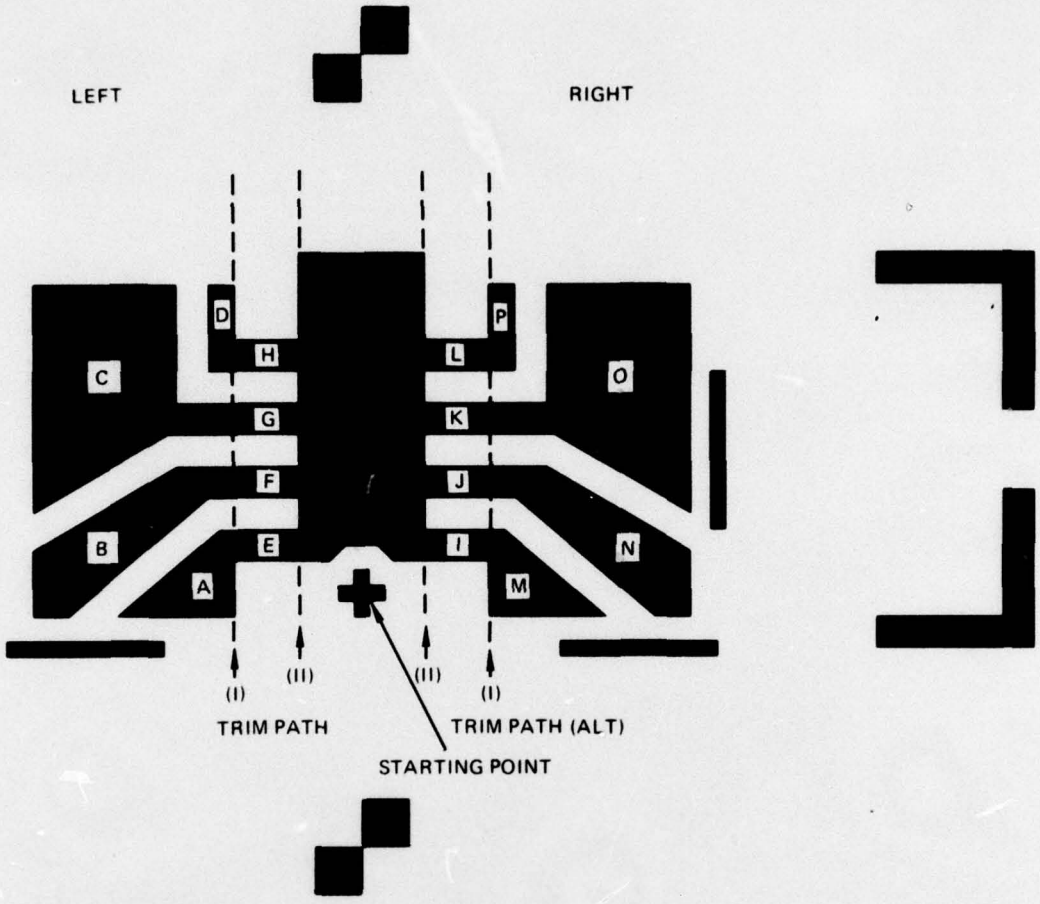
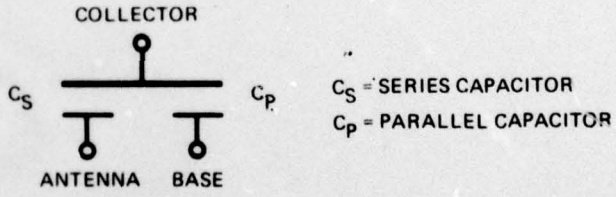
[1] a) All antennas formed incorrectly.
b) Some of these units had poor hole-pattern registration. Both problems however, are relatively minor.



A.) UPPER PLATE ARTWORK



B.) ELECTRICAL SCHEMATIC

Figure 1. Trimmable Capacitor Pattern (Binary Ratio)

Figure 1-a shows the upper plate pattern of the "Experimental-Design" only. The lower plates are located under plates (A+B+C+D) and (M+N+O+P), respectively.

These lower plates are continuous and extend beyond the outside perimeter of each upper plate by about 0.015 inches so that slight pattern misalignment will not substantially effect individual bit capacities.

The Dual-Box and outer line patterns, shown in figure 1-a, are used only for registration of upper to lower plates during fabrication and are not part of the final product.

Differential capacitance measurements were made on six "Experimental Fringing" design samples, plus several "Theoretical Fringing" design samples during this quarter. Of the two basic approaches, the "Experimental Fringing" design came closest to the desired values of capacitance on an overall basis. A Hewlett-Packard capacitance bridge (Model 4270A) was used for these measurements in conjunction with a test fixture whose residual capacitance was stable and accurately known. Measurements were conducted in an air conditioned environment to assure controlled, reproducible results.

Both lower plates of each test capacitor were connected to one side of the test fixture. The top plate was then attached from the central bar to the opposite fixture plate using a short ribbon lead to minimize inductance. Individual capacitor plates were then removed by cutting the gold linking "street" along "TRIM PATH (I) - LEFT", "TRIM PATH (II) - LEFT", "TRIM PATH (ALT) (I) - RIGHT" and "TRIM PATH (ALT) (II) - RIGHT", respectively (as shown in figure 1-a). This was done, one element at a time, so that readings before and after a cut represented the capacitance bit removed (i.e., cutting "street" E along TRIM PATH (I) - LEFT determines the capacitance value of bit A by subtracting pre- and post- cut readings).

The results of these experiments are summarized in table 4 for the six "Experimental Fringing" designed capacitors.

Table 4. Test Results of "Experimental-Fringing" Chip Capacitors[A]

SIDE	CAPACITOR DESIGNATION	DESIRED VALUE (pfd)	AVERAGE MEASURED VALUE (pfd)	% ERROR OF MEAN	LIMITS - % ERROR MAXIMUM	MINIMUM	TOTAL SPREAD
LEFT	D	0.1533	0.151	-1.50	+16.1	-10.0	26.1
	A	0.3066	0.258	-15.85	-10.0	-22.4	12.4
	B	0.6132	0.598	-2.48	+1.8	-9.0	10.8
	C	1.2264	1.280	+4.37	+7.7	-1.3	9
RIGHT	P	0.1533	0.138	-9.98	+3.4	-24.4	27.8
	M	0.3066	0.253	-17.48	-19.8	-14.9	4.9
	N	0.6132	0.598	-2.48	+2.7	-10	12.7
	O	1.2264	1.284	+4.70	+7.0	+1.8	5.2

A) Based on a sample of six units.

The average street capacitance was measured to be 0.056 pfd with a standard deviation of 0.019 pfd. The residual capacity of the upper-plate central bar to each lower plate was 0.630 pfd, including streets.

The large spread in street capacitance is probably the result of their small size and that there is no bottom plate immediately under each street.[2] An additional problem contributing to this variation is the method of cutting the streets. In all cases, this was accomplished by hand cutting using a diamond-tipped scribe. It was quite difficult to cut an individual street at a specific location along either "TRIM PATH" with any degree of consistency. This probably contributes to the comparatively large variations in the small bit capacitors (D&P).

[2] Street capacitance is principally composed of energy stored in the fringing fields from street to lower plates.

The results summarized in table 4 indicate that the basic chip capacitor design is not far from the desired values (except possibly capacitor A and M). In fact, minor changes in pad sizes (including A and M) will shift their mean capacities to the desired values without a major physical modification to pad sizes. Before committing to a final design, however, two remaining potential problems will be investigated.

The first problem deals with the stray capacitance from upper plate pads to the oscillator pcb and disc after the antenna is installed on the Oscillator Disc Assembly (Dwg No. 06006414). (See figure 2.) This problem, in effect, is similar to placing one's hand near a small capacitor while measuring its value. Since the desired pad capacities are small, minor perturbations in existing electric field configurations, or extra capacity to ground, could change individual pad size.[3] Preliminary tests were conducted to verify this by measuring overall capacitance (with pads attached) and mounting the chip capacitor to a formed antenna alone, then attaching a disc assembly. Differences in overall capacitance varied from 0.090 to 0.160 pfd in both shunt or series capacity. How much of this change is the result of extra capacity from the upper plate pads, and how much is due to the central connecting bar and streets will be determined in the next quarter.

The second problem, inconsistencies in pad capacitances due to the method used for cutting the streets and attaching the pads to the main plate, was discussed above.

Present plans are to assemble several formed antennas with representative chip capacitors and mounting these units in oscillator assemblies (excluding transistor, chokes, diode, and resistor).

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[3] A fixed increase in overall capacitance is no problem since it can be compensated by removing a similar amount from the epoxy-glass antenna.

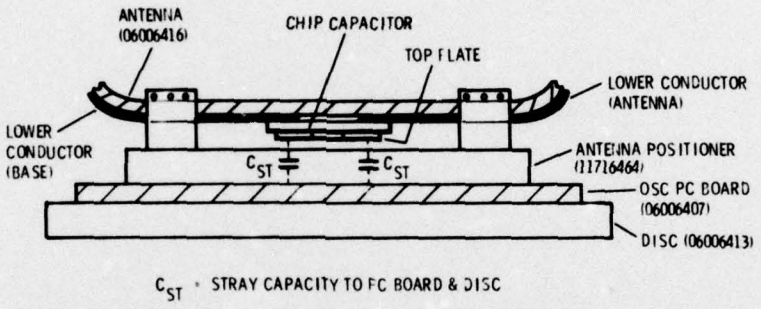

Figure 2. Partial Side View of Oscillator Assembly (Dwg No. 06006415)

Then, accurate differential capacity measurements will be made in a similar manner to the above measurement techniques using a laser to cut the streets. This added effort is to assure proper capacitance step size in the overall oscillator assembly.

2.2.4 Chip Capacitor Resolution

The above goal capacitance values are extremely small. Measurement is also tricky.[4] To bring this into perspective, a short discussion of the needed resolution in oscillator sensitivity is in order.

The design goal of this program is to test and trim oscillator assemblies to a specified value $\pm$.5 percent (i.e., for a sensitivity of 100 mVrms, $\pm$.5 percent represents $\pm$0.5 mVrms). The present HDL oscillator design has a sensitivity-capacity slope that is in the range of 0.024 pfd/mVrms on the average. This implies a maximum least significant bit (LSB) of 0.012 pfd, about an order of magnitude lower than the design LSB.[5] To obtain this resolution, a second and possibly third cut will be necessary that are continuous providing a needed infinite resolution.

Present plans are to provide a step-wise cut on first tuning using the binary capacitors. The second and third trials will be continuous. If convergence is assumed, the second and third trials should have smaller differential capacitance changes allowing for removal of smaller portions of a remaining pad or street. An alternate approach is to modify the existing design to add a fifth pad (of about 0.2 pfd) to each capacitor in the area of the laser cross hairs, which can be used for continuous cutting. In effect, this fifth pad will serve as the vernier capacitances used on second and third tuning trials.

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[4] LEC has relied entirely on differential capacitance measurements with a bridge capable of a 0.001 pfd resolution. The consistency of measurements to date can be estimated by a close evaluation of the data in table 4.

[5] This also assumes that measurement accuracy is infinitely good.

A final design will be available at the end of the next quarter.

2.3 TEST SIGNAL SUBSYSTEM

Figure 3 shows an expanded block diagram of the rf modulator that processes rf energy from test oscillators. A description of its operation was presented in the Fourth Quarterly Report.

This revised diagram (figure 3) includes additional level setting attenuators in the signal circuit, BITE equipment to independently check critical modulator functions, and an automatic means of setting oscillator power supply voltage via the computer. This latter power supply is used as the principal power source to both oscillator (Dwg No. 06006415) and amplifier assemblies (Dwg No. 06006401 and -04). This power supply is an extremely low-noise, stable, resistor programmable source that will be switched automatically from the oscillator test fixture to the amplifier board fixture, as required via computer command. Note that two voltage values are needed depending upon whether the oscillator or amplifiers are to be trimmed. The oscillator assemblies require a +27.250-Vdc source, whereas the amplifier boards require +30.000 Vdc. The single supply will accurately provide both levels.

A minor circuit change was made to eliminate one directional coupler from the original concept. (See figure 5 of the Fourth Quarterly Report.) This was removed to reduce cost and improve the residual vswr between the Load Chamber and Port 2 of the input circulator.

Separate low-pass filters had also been considered for use in the "Signal Separate, Scale, and Filter" Block (Block 1) to minimize error signals introduced by the single-sideband modulator (Block 13). Only the mid-band filter[6] will now be installed since amplifier trimming is accomplished using a 720-Hz constant level burst only. However, space will be allotted to expand the processing

[6]Passing 720-Hz signals, but rejecting higher order products.

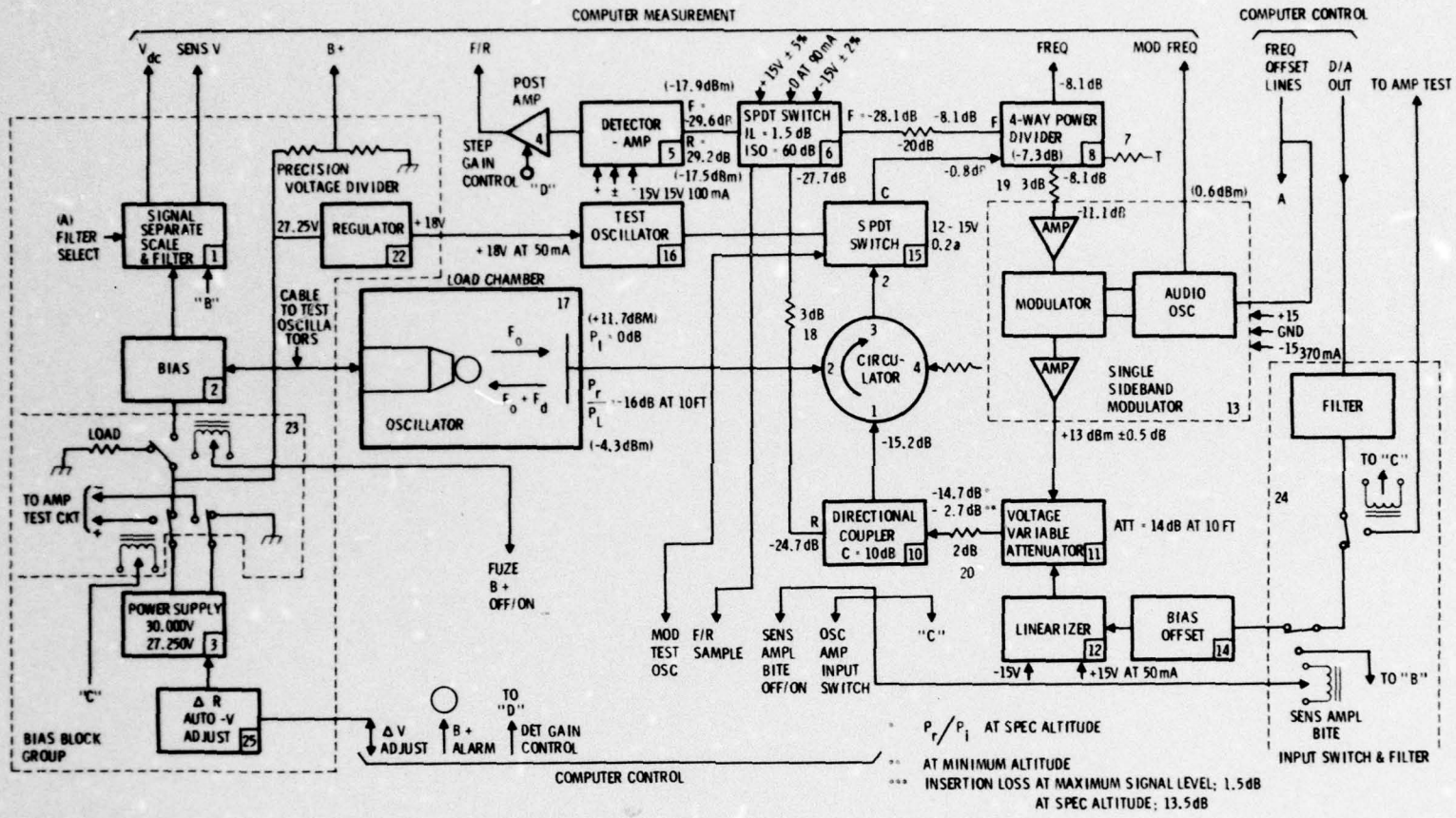

Figure 3. Modulator ECOM, Fuze

circuitry if required for operation at 240 and 1600 Hz. This step was also taken to reduce the cost of the processing unit. The reduction in capability in no way affects the present program goals.

2.3.1 RF Modulator Status

Twenty-five major blocks are shown in figure 3. Nine are designed by LEC with the remaining 16 as purchased items. All have been ordered along with additional components such as semi-rigid line and rf connectors.

2.3.1.1 *Purchased Components.* - Of the 16 purchased items, 12 have been received along with the rf connectors. The remainder are scheduled for delivery during the beginning of the next quarter[7].

2.3.1.2 *In-House Designs.* - The Load Chamber is actually completed except for the final design of the pickup probe. The oscillator test fixture has been wired on the load side, along with a temporary connector for access to the test fixture. A *temporary* means of stimulating test oscillators has also been installed in lieu of the actual modulator. This technique uses a passive spinning dipole in place of the pickup probe. The spinning dipole returns part of its induced signal to the unit under test, simulating ground returns. This alternate technique is presently used for production testing of M732 oscillators. The method provides an interim means of testing prototype oscillators before rf modulator installation. Both synchronous motor and dipole have been installed for this function.

Bias Block Group. - Blocks 1, 2, 3, 22, 23, and 25 are being designed as a group and will be mounted in close proximity to the Load Chamber test fixture.

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[7] Including the single-sideband modulator (Block 13).

The purpose of this group is to provide power to the units under test and extract, scale, and filter detector and sensitivity voltages for measurement by the computer a/d converter. Locating these units near the oscillator test fixture at the Load Chamber minimizes the problem of 60-Hz pickup and ground loops[8].

Signal scaling is incorporated to adjust maximum signal levels to about 10V peak in order to minimize errors in measurement caused by the resolving power of the HP a/d converter (an LSB = 5mV).

Figure 4 shows the breadboard circuitry of the Bias and Signal Separate, Scale, and Filter blocks (1 and 2). This diagram is simplified in that it does not show supply voltage connections, offset bias adjustments, guard, or BITE circuits. Power supply (Block 3) switching circuits are designed but not shown.

The oscillator bias section applies appropriate voltages to the test oscillator through shielded leads to the oscillator test fixture. The input voltage follower (Harris Part No. HA2645) is a stable, unity-gain, high-level impedance transformer that isolates the oscillator bias circuits from the signal sensing circuits. A separate 60V supply powers this stage allowing for signal input levels exceeding 40V, which is the maximum expected dc input level. The output of this stage is split into ac and dc signal processing circuits.

A temperature-stable resistive voltage divider, active low-pass filter, and line driver reduce the dc detector voltage to about one quarter of its actual value. The overall gain is precisely set and stable. AC detector voltage perturbations are removed by a four-pole low-pass active filter. A line driver is also incorporated to feed the computer multiplexer and a/d converter. This latter unit is located in the computer cabinet, which is about ten feet from the Bias Block Group.

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[8] Principally on the detector output line, which is relatively high impedance.

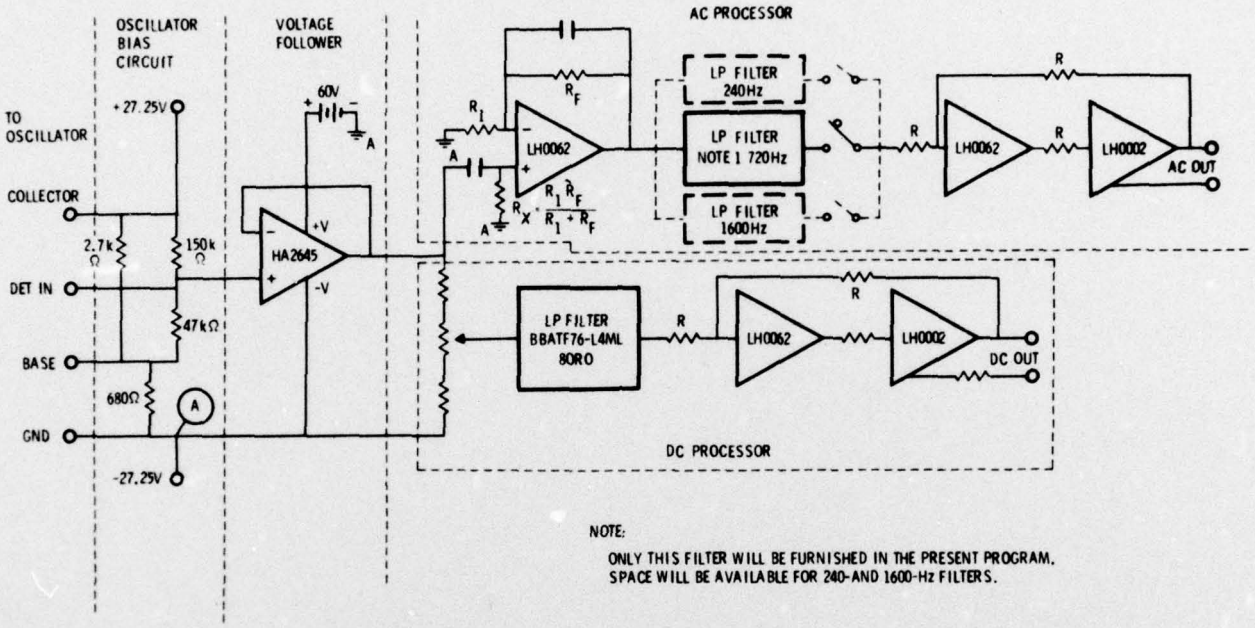

Figure 4. Bias Block Group, Breadboard Circuitry

AC signal perturbations are amplified and filtered by a 720-Hz active filter to minimize higher order outputs from the rf modulator single-sideband generator[9]. The dotted 240- and 1600-Hz filters and switching network will not be incorporated for this program, however, provisions will be made for expansion. Each output is selectable by the computer depending on the desired offset frequency. A line driver feeds the computer multiplexer and a/d converter.

The paper design of this section is in progress. A breadboard of the unit will be constructed and tested during the next quarter.

Post Amplifier, Bias Offset, Input Switching, and Filter Group. - Designs for these circuits will begin in the next quarter.

Present plans are such that the rf modulator circuitry should be finalized and tested by the end of the next quarter.

2.3.2 Amplifier Board Signal Processing

The present program requires testing and trimming of M732 oscillators and amplifiers, separately. The previous discussion concentrated on testing oscillators only. The following discussion focuses on the amplifier board signal processing circuitry. Figure 5 shows a block diagram of the amplifier board signal circuits. Presently, production amplifiers are tested individually by stimulating each unit with an audio M-wave at its input. The present program dispenses with this approach by stimulating these units with short bursts of constant level audio, while making use of FFTs to determine the unit's transfer function. Gain adjustment is made by varying R9 using laser trimming.

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[9] Additional filtering is provided analytically by use of an FFT on the resulting output. Although this breadboard incorporates an active filter, the final version may rely entirely on the FFT to separate fundamental from spurious signals.

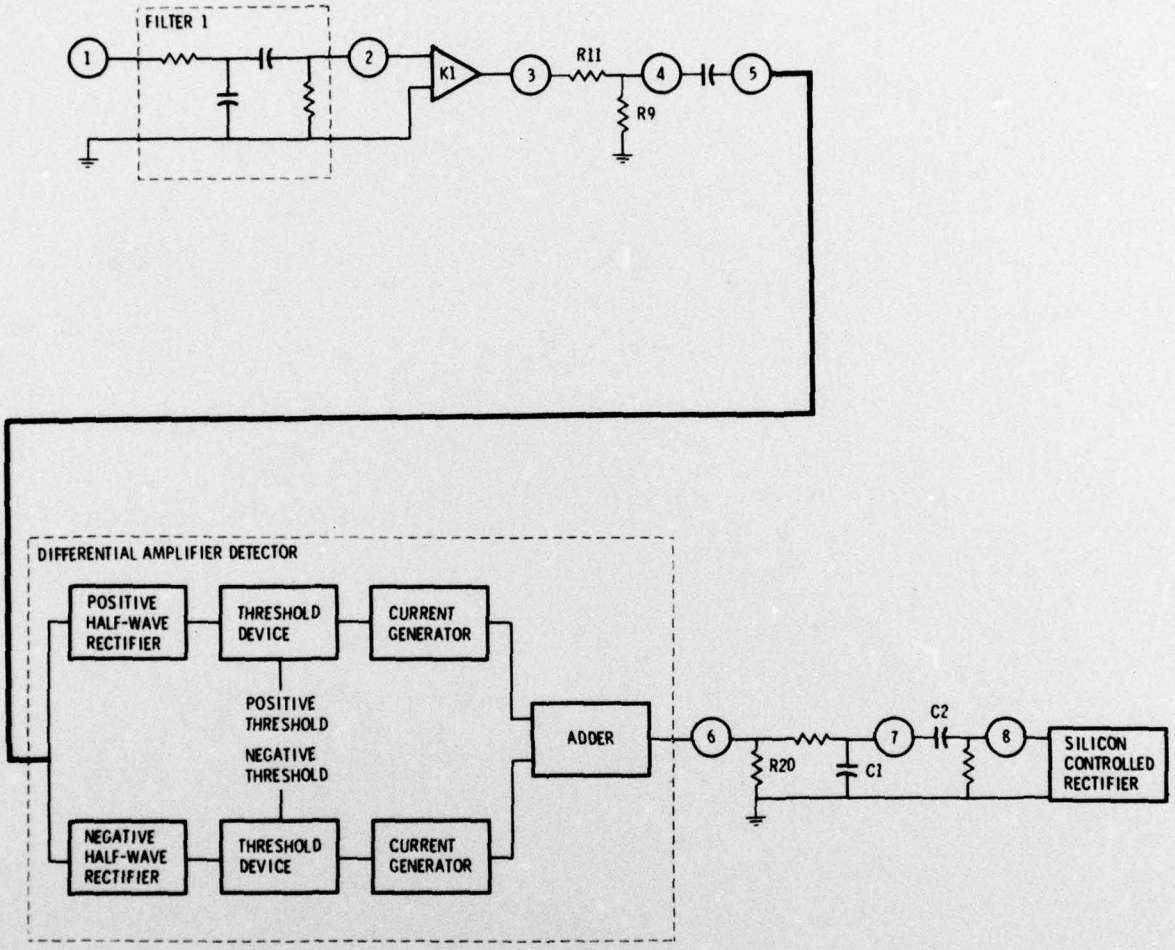

Figure 5. Amplifier Block Diagram

To accomplish this, several sampling points are needed in the signal path, along with a means of rapidly initializing selected capacitors so that they return to their quiescent voltages before test.

Figure 5 shows the test points in the signal circuits. Figure 6 presents the bias, energy storage, and fire pulse output circuitry also on the amplifier board. A fire pulse output voltage sensing circuit is also needed to determine the scr firing voltage at the leading edge of the fire pulse output. This last sensing point is shown in figure 6, although it is considered an added output test point.

In all, nine signal test points are needed, eight in the direct signal path (figure 5), and one sensing the onset of the fire pulse output (figure 6). This latter point triggers a constant amplitude one-shot, which drives the Event Sense card in the computer.

Three capacitors must be rapidly initialized to their quiescent voltage values before any given test. These capacitors are:

- C_1 - The integrator capacitor.
- C_2 - SCR coupling capacitor.
- C_{16} - Fire pulse energy storage capacitor.

C_1 and C_2 are shown in figure 5. C_{16} is shown in figure 6. The "Quick-Charge Circuit" block shown, recharges C_{16} to its quiescent state between individual tests. The relays shunting C_1 and C_2 are used to discharge C_1 and C_2 before the beginning of a test.

Since the signal circuit source and load impedances are relatively high, a voltage follower will have to be used to isolate the pickup circuits from the signal path circuitry. Several requirements must be met by these test probe circuits. They are as follows:

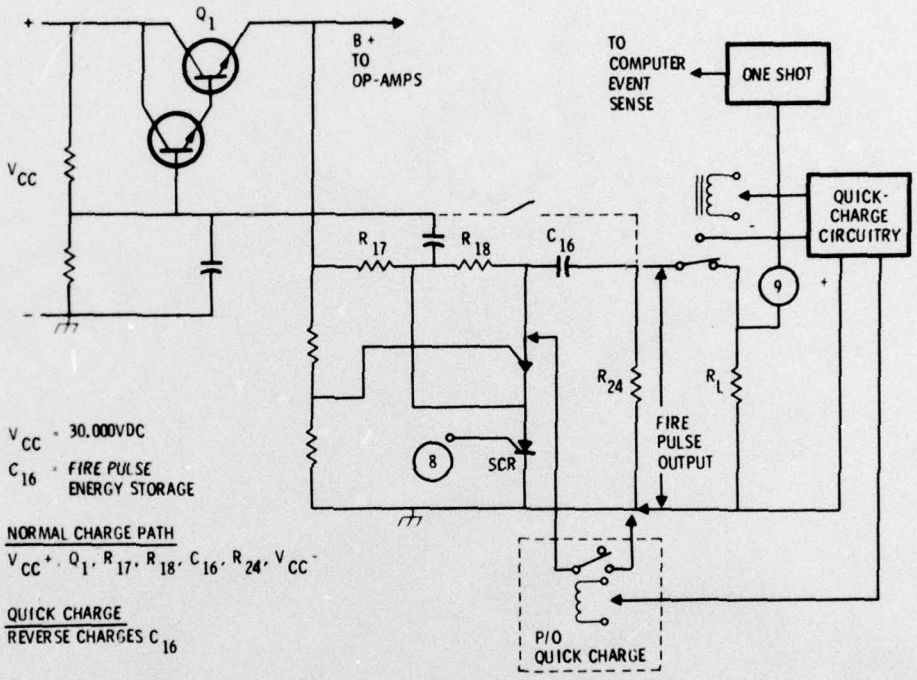

Figure 6. Amplifier Board Bias and Fire Pulse Circuits

- Isolation of signal from the pickup circuits.
- Gain.
- Minimization of 60-Hz pickup.
- Minimization of ground loops.

Item (1) is needed to assure that the test probes do not interfere with normal amplifier operation. Item (2) is needed to increase the low-level test signals to about 10V peak reducing a/d converter resolution errors and minimizing the effect of 60-Hz pickup. The latter two items are needed to assure a minimum error signal resulting from ground loops pickup on the lines connecting each output to the computer multiplexer.

Two possible circuit approaches are being considered. One approach is to use an op-amp with high differential and common mode input impedance (i.e., National LH0062CD) along with low bias current and voltage offset. This unit can be used as a unity-gain non-inverting voltage follower feeding a line driver circuit similar to that shown in figure 5.

The alternate approach incorporates a Burr-Brown Iso-Op-Amp, such as a Model 3451, in a similar circuit. This latter approach has the added advantage of physically and electrically isolating the computer ground from the analog output grounds, thus reducing ground loop pickup.

Design and breadboard testing of the amplifier pickup and quick-charge circuitry will be completed by the end of the next quarter.

2.4 MECHANICAL DESIGN

During this report period, most of the outstanding tasks have been solved. A cabinet has been ordered that will house the modulator, laser control, and the interface panels.

Interface connector panels, laser safety shield modifications, and the nest for the amplifier assembly needed to hold down the amplifier while laser trimming have been completed. (See figures 7 and 8)

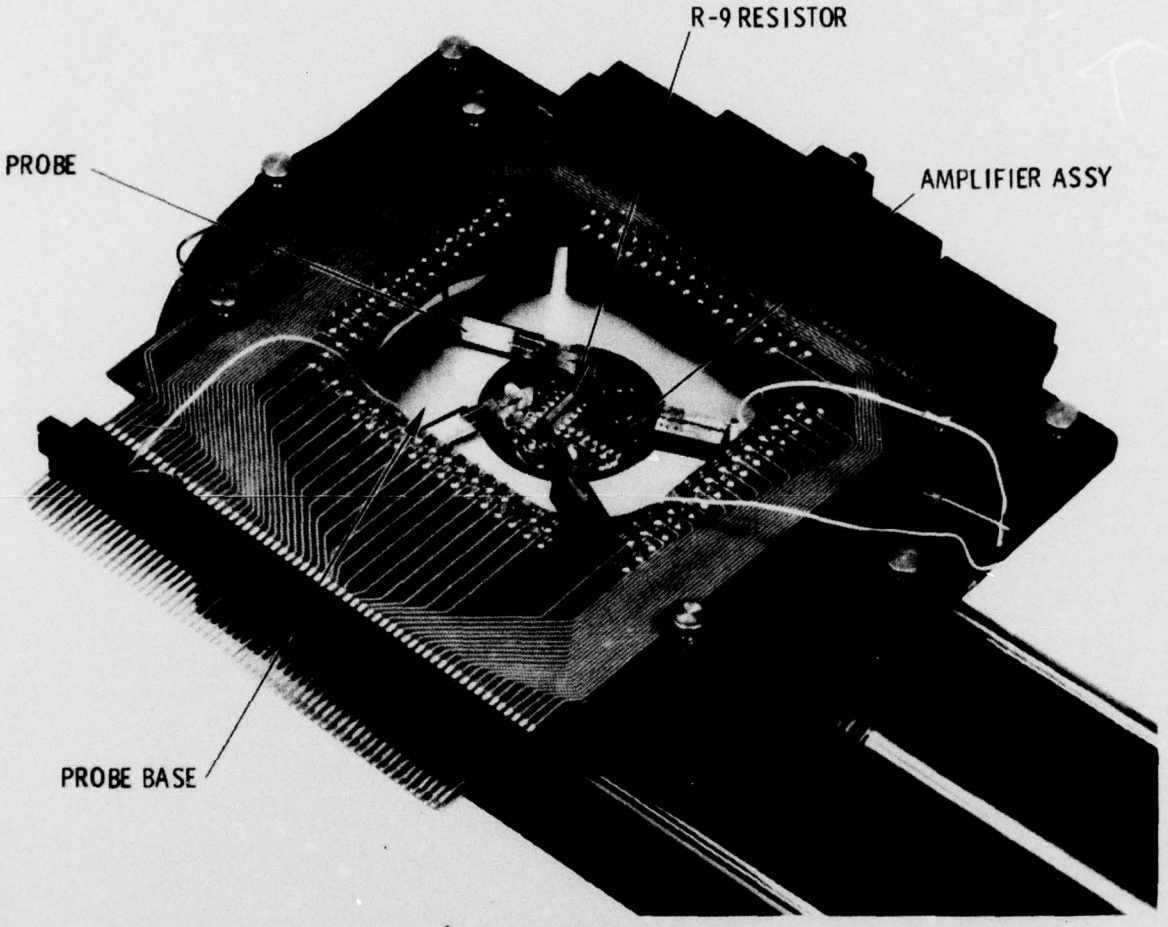

Figure 7. Amplifier Assembly Laser Trimming and Probing Position

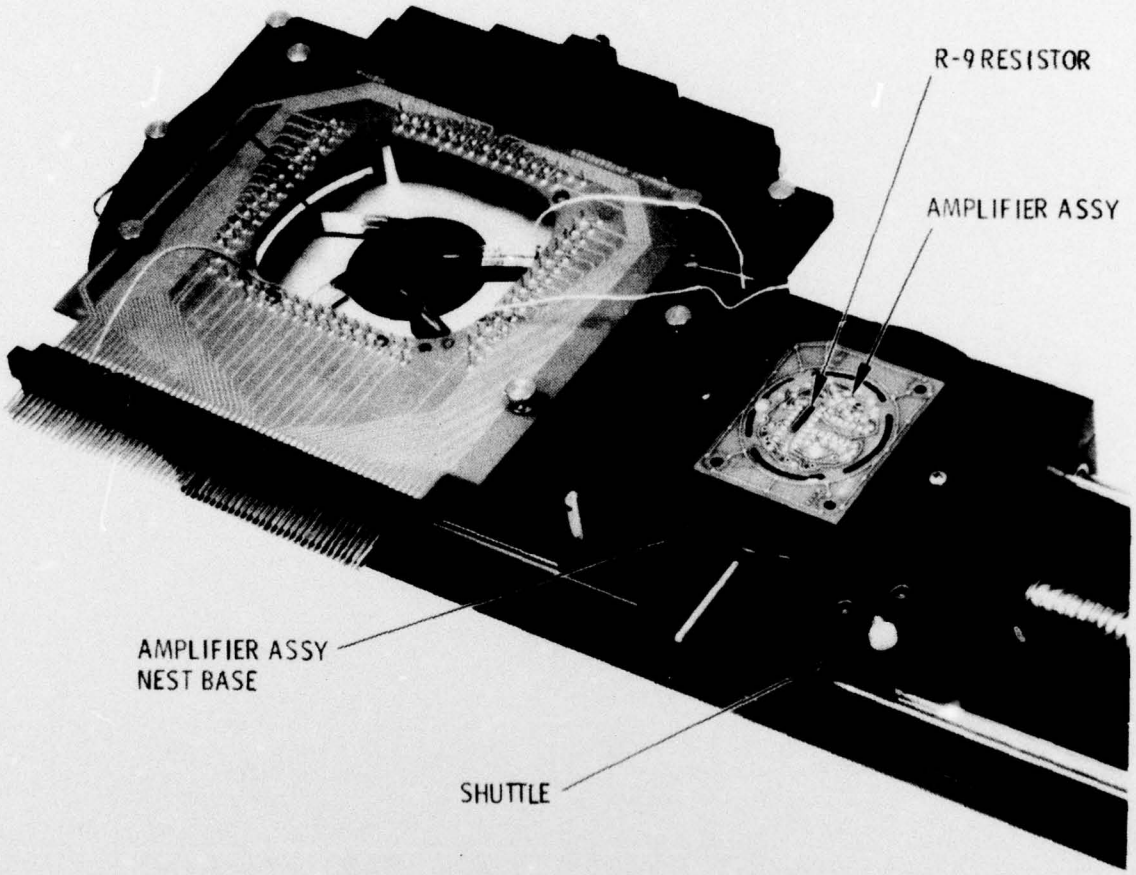

Figure 8. Amplifier Assembly Nest - Unloading Position

To facilitate the probing of the amplifier assembly, 12 pads have been added to the amplifier pcb to assure a superior probe contact.

2.5 PROGRAMMING

The simulation of the real-time amplifier program was completed. This program was described in the previous quarterly report. The flow chart shown in figure 9 is repeated here for reference purposes.

In this quarter, the simulation program was modified so that it could be used for the actual real-time program for testing oscillators. It was then actually run and debugged on the ECOM test stand. The preliminary results indicate that the program can be used with only minor modifications. The i/o routines will, of course, have to be added to the program. These i/o routines have been written and are presently being debugged. Some initial problems with the i/o were encountered because of the particular idiosyncrasies of the computer. However, these problems have now been corrected and debugged. Computer control of the laser was achieved. Additionally, it was determined that the program could not fit into the original 33k memory. Either program segmenting and overlaying or additional memory could be used to overcome this problem. It was decided that it would be preferable to obtain the additional memory since this would provide a permanent upgrading of the system. An additional 32,000 words have been ordered and are expected to be delivered at the beginning of the sixth quarter. In addition, a more complex operating system (i.e., RTE-III) will be installed along with the additional memory. This too will provide an upgrading of the system since it will allow for multiprogramming.

In this upcoming quarter, it is expected that the i/o routines and the main line amplifier test program will be merged, debugged, and tested with the amplifier units.

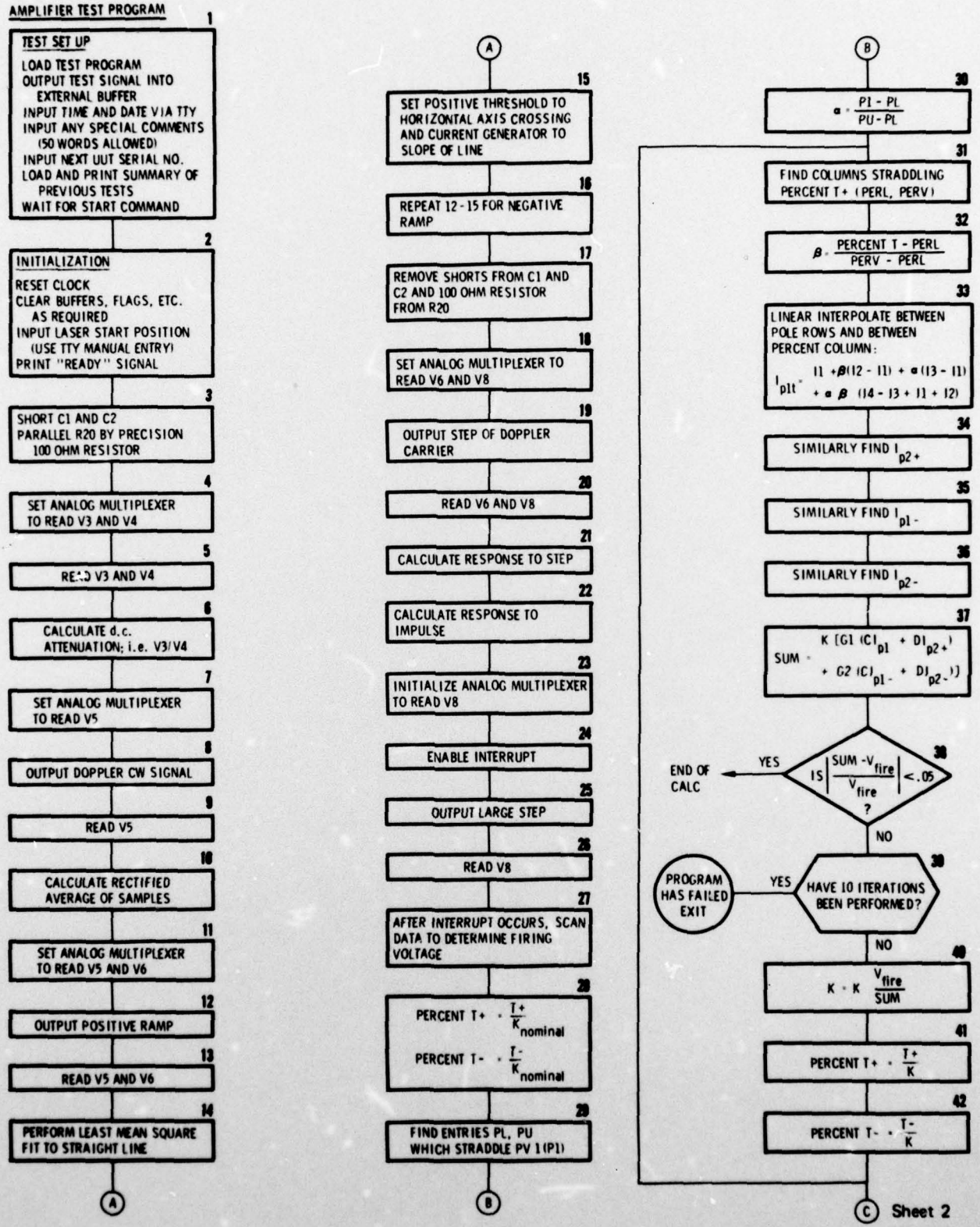

Figure 9. Amplifier Test Program (Sheet 1)

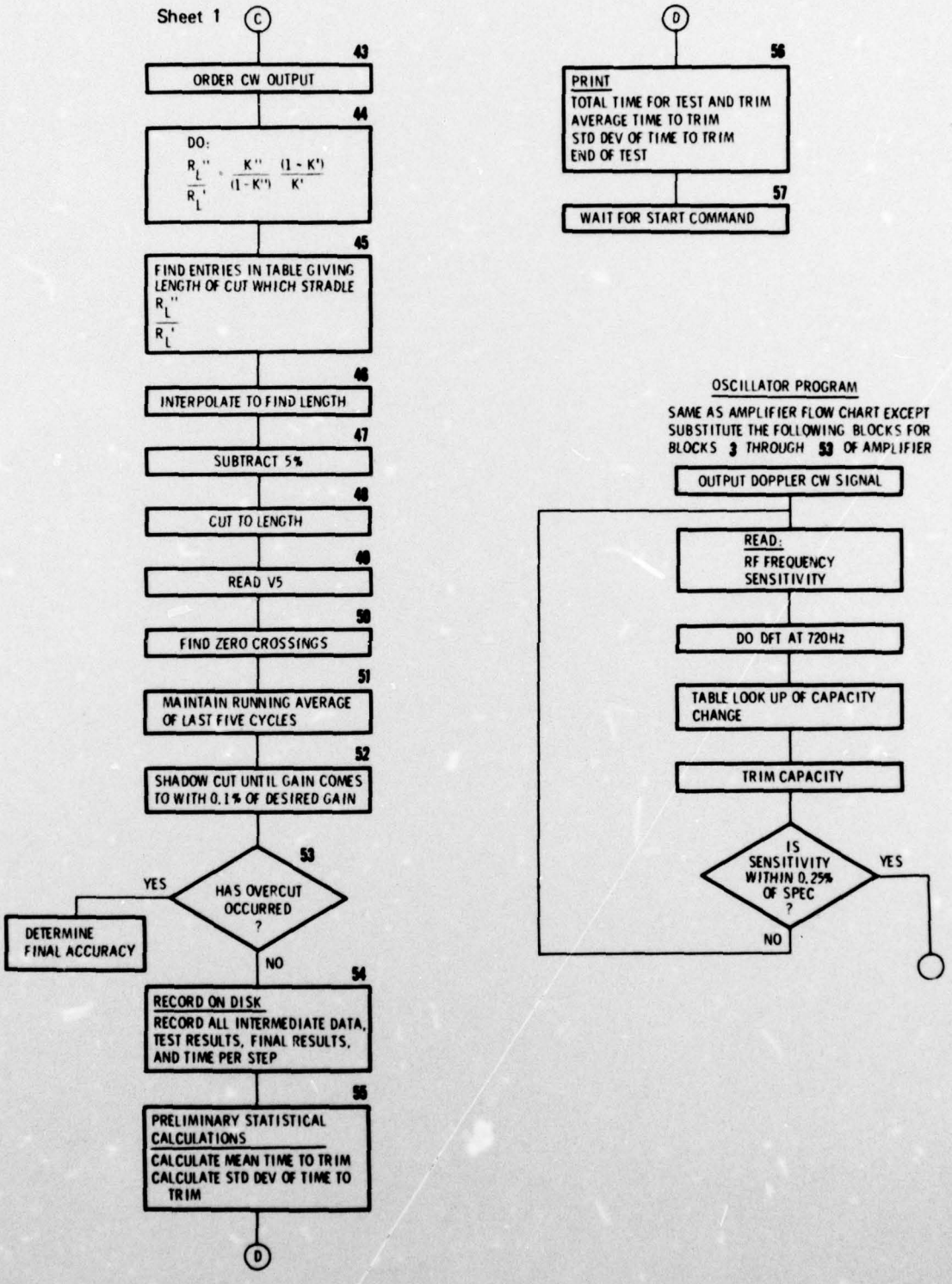

Figure 9. Amplifier Test Program (Sheet 2)

3. CONCLUSION

Objectives of the fifth quarter were met as follows:

- The amplifier simulation program was incorporated into the real-time program.
- System integration was completed (with the exception of the oscillator test signal system).
- Seventy-five amplifiers were built and tested.
- Seventy-five oscillator assemblies were built.
- Components for the oscillator test signal subsystem were ordered.

4. PROGRAM FOR NEXT QUARTER

During the next reporting period, the following activities are planned:

- Additional memory (32k) and a sophisticated operating system will be installed into the computer.
- The real-time amplifier test prcgram will be debugged and tested with the prototype amplifier.
- The real-time oscillator program will be written.
- The oscillator test signal subsystem will be built.
- Amplifier and oscillator contruction will continue.

5. PERSONNEL

During this reporting period, the following personnel worked on this program for the number of hours indicated.

Name	Program Function	Hours
A. J. Eisenberger	Program Manager	71
P. Kaszerman	System Engineer	160
R. F. De Mattos	Tester RF and Fuze	290
T. R. Griffin	Fuze Microcircuits	108
H. J. Curnan	Laser Trimmer and Fuze Microcircuits	78
S. Conston	Digital Components	164
U. Z. Escoli	Mechanical Design	178
A. H. Owens	Mechanical Design	128
R. Boroson	Programmer	384
	Draftsmen, Machinist, Technical Publications, etc.	858

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Laser Trim
Computer Test
Functional Test

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

During the fifth quarter, the amplifier test simulation program was modified and incorporated into the real-time program. Input/output routines were added and partially debugged. Computer control of the laser was achieved. An additional memory (32k) and a more sophisticated operating system were ordered for the computer.

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